

## WHAT IS CLAIMED IS:

1. A data processor comprising:

C execution clusters, each of said C execution clusters comprising an instruction execution pipeline having N processing stages capable of executing instruction bundles comprising from one to S syllables, wherein each said instruction execution pipelines is L lanes wide, each of said L lanes capable of receiving one of said one to S syllables of said instruction bundles;

an instruction cache capable of storing a plurality of cache lines, each of said cache lines comprising C\*L syllables;

an instruction issue unit capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward said C execution clusters; and

alignment and dispersal circuitry capable of receiving said complete instruction bundles from said instruction issue unit and routing each said received complete instruction bundles to a correct one of said C execution clusters as a function of at least one address bit associated with each of said complete instruction bundles.

1           2.    The data processor as set forth in Claim 1 wherein said  
2 alignment and dispersal circuitry routs each said received complete  
3 instruction bundles to said correct execution cluster as a function  
4 of at least one address bit associated with at least one syllable  
5 in said each complete instruction bundle.

1           3.    The data processor as set forth in Claim 1 wherein said  
2 alignment and dispersal circuitry routes each received complete  
3 instruction bundles to said correct execution cluster as a function  
4 of a cluster bit associated with each complete instruction bundle.

1           4.    The data processor as set forth in Claim 1 wherein said  
2 alignment and dispersal circuitry routs each said received complete  
3 instruction bundles to said correct execution cluster as a function  
4 of a stop bit associated with at least one syllable in said each  
5 complete instruction bundle.

1           5.    The data processor as set forth in Claim 1 wherein said  
2 alignment and dispersal circuitry comprises multiplexer circuitry  
3 capable of routing said each received complete instruction bundle  
4 to any one of said C execution clusters.

1           6.    The data processor as set forth in Claim 5 wherein said  
2 alignment and dispersal circuitry comprises control logic circuitry  
3 capable of controlling said multiplexer circuitry.

1           7.    The data processor as set forth in Claim 6 wherein said  
2 control logic circuitry controls said multiplexer circuitry as a  
3 function of at least one of:

4           1) said at least one address bit associated with said  
5 each complete instruction bundle;

6           2) at least one address bit associated with at least one  
7 syllable in said each complete instruction bundle; and

8           3) a cluster bit associated with said each complete  
9 instruction bundle.

10          8.    The data processor as set forth in Claim 1 wherein  $L=4$ .

11          9.    The data processor as set forth in Claim 1 wherein  $C=3$ .

1           10. A processing system comprising:  
2           a data processor;  
3           a memory coupled to said data processor;  
4           a plurality of memory-mapped peripheral circuits coupled  
5 to said data processor for performing selected functions in  
6 association with said data processor, wherein said data processor  
7 comprises:

8           C execution clusters, each of said C execution  
9 clusters comprising an instruction execution pipeline having  
10 N processing stages capable of executing instruction bundles  
11 comprising from one to S syllables, wherein each said  
12 instruction execution pipelines is L lanes wide, each of said  
13 L lanes capable of receiving one of said one to S syllables of  
14 said instruction bundles;

15           an instruction cache capable of storing a plurality  
16 of cache lines, each of said cache lines comprising C\*L  
17 syllables;

18           an instruction issue unit capable of receiving  
19 fetched ones of said plurality of cache lines and issuing  
20 complete instruction bundles toward said C execution clusters;  
21 and

22           alignment and dispersal circuitry capable of

23 receiving said complete instruction bundles from said  
24 instruction issue unit and routing each said received complete  
25 instruction bundles to a correct one of said C execution  
26 clusters as a function of at least one address bit associated  
27 with each of said complete instruction bundles.

1 11. The processing system as set forth in Claim 10 wherein  
2 said alignment and dispersal circuitry routs each said received  
3 complete instruction bundles to said correct execution cluster as  
4 a function of at least one address bit associated with at least one  
5 syllable in said each complete instruction bundle.

1 12. The processing system as set forth in Claim 10 wherein  
2 said alignment and dispersal circuitry routs each said received  
3 complete instruction bundles to said correct execution cluster as  
4 a function of a cluster bit associated with said each complete  
5 instruction bundle.

1           13. The processing system as set forth in Claim 10 wherein  
2 said alignment and dispersal circuitry routs each said received  
3 complete instruction bundles to said correct execution cluster as  
4 a function of a stop bit associated with at least one syllable in  
5 said each complete instruction bundle.

1           14. The processing system as set forth in Claim 10 wherein  
2 said alignment and dispersal circuitry comprises multiplexer  
3 circuitry capable of routing said each received complete  
4 instruction bundle to any one of said C execution clusters.

1           15. The processing system as set forth in Claim 14 wherein  
2 said alignment and dispersal circuitry comprises control logic  
3 circuitry capable of controlling said multiplexer circuitry.

1           16. The processing system as set forth in Claim 15 wherein  
2           said control logic circuitry controls said multiplexer circuitry as  
3           a function of at least one of:

4                 1) said at least one address bit associated with said  
5           each complete instruction bundle;

6                 2) at least one address bit associated with at least one  
7           syllable in said each complete instruction bundle; and

8                 3) a cluster bit associated with said each complete  
9           instruction bundle.

10           17. The processing system as set forth in Claim 10 wherein  
11           L=4.

12           18. The processing system as set forth in Claim 10 wherein  
13           C=3.

1           19. For use in a data processor comprising C execution  
2 clusters, each of the C execution clusters comprising an  
3 instruction execution pipeline having N processing stages capable  
4 of executing instruction bundles comprising from one to S  
5 syllables, wherein each the instruction execution pipelines is L  
6 lanes wide, each of the L lanes capable of receiving one of the one  
7 to S syllables of the instruction bundles, a method of routing  
8 instruction bundles into the L lanes in the C execution clusters  
9 comprising the steps of:

10           fetching cache lines from an instruction cache, each of  
11 the cache lines comprising C\*L syllables;

12           issuing complete ones of the instruction bundles toward  
13 the C execution clusters; and

14           routing each the received complete instruction bundles to  
15 a correct one of the C execution clusters as a function of at least  
16 one of:

17           1) the at least one address bit associated with the  
18 each complete instruction bundle;

19           2) at least one address bit associated with at least  
20 one syllable in the each complete instruction bundle; and

21           3) a cluster bit associated with the each complete  
22 instruction bundle.



1           20.   The method as set forth in Claim 19 wherein L=4 and C=3.